one of N operation modes, and operates in said one of N operation modes, said semiconductor device comprising:

a selection circuit for selecting an operation mode from said N operation modes when said input signal indicates said operation mode, and for selecting a predetermined operation mode from said N operation modes when said input signal is an undefined signal indicating none of said N operation modes;

a core circuit for storing data; and

a control circuit operating in one of said [an] operation mode and said predetermined operation mode selected by said selection circuit to control said core circuit,

wherein selection of said predetermined operation mode prevents malfunction of said control circuit ~~said internal circuit~~ when said input signal is said undefined signal.

Claim 6, line 9, after "said", insert --predetermined--.

Claim 7, line 5, delete "internal" and insert therefor --control--; and

line 6, delete "internal" and insert therefor --control--.

REMARKS

The Office Action dated November 28, 1997 has been received and carefully noted. The above amendments, and the following remarks, are submitted as a full and complete response thereto.

The drawings have been amended to be in compliance with United States patent practice. The specification and title have been amended to more clearly describe the

subject matter of the invention. Claims 1-11 have been amended as appropriate to more particularly point out and distinctly claim the subject matter of the invention. No new matter has been added. Claims 1-11 are respectfully submitted for consideration.

The drawings were objected to on the grounds that Figures 1A - 1D, 2 and 5 were not properly indicated as being prior art. Attached is a Request for Approval of Drawing Changes, wherein Figures 1A - 1D, 2, and 5 have been amended as shown in red. Upon approval of this request, formal drawings will be timely filed.

The specification was objected to as having minor informalities therein. Applicant appreciates the Examiner's courtesy in highlighting these informalities, and respectfully submits that the specification has been amended as appropriate to be in compliance with United States patent practice.

The title of the invention was objected to as not being adequately descriptive of the claimed invention. The original title of the invention has been deleted, and a new title is submitted which is more clearly directed to the subject matter of claims 1-11.

Claims 2-4 and 6-11 were rejected under 35 USC § 112, second paragraph, as being indefinite. The Office Action took the position that these claims contained unclear or misdescriptive terms. Applicant submits that these claims, as submitted herein, particularly point out and distinctly claim the subject matter of the invention.

Claims 9-11 were separately rejected under 35 USC § 112, second paragraph, as being incomplete for omitting essential steps. The Office Action took the position that the claims were inoperative in that the steps of selecting, detecting, storing, or holding information regarding an operation mode were incomplete. Applicant respectfully traverses

this rejection, and submits that the claims do not recite "only an input signal". All of claims 9-11 recite methods of selecting an operation mode using an input signal. There is no requirement in any of these claims that it is only an input signal which is used to select an operation mode. It is respectfully submitted that these claims particularly point out and distinctly claim the subject matter of the invention based upon the disclosure thereof in the specification. As noted previously, the claims recites steps of selecting, detecting, storing, or holding information regarding an operation mode based upon a condition of an input signal. It is respectfully submitted that there is no requirement or recitation in the claims that there be "no other input" to the semiconductor device. Applicant therefore respectfully submits that claims 1-11 particularly point out and distinctly claim the subject matter of the invention, and are in compliance with United States patent practice.

Claims 1 and 5 were rejected under 35 USC § 102(b) as being anticipated by Toda (U.S. Patent No. 4,984,216). Applicant respectfully submits that these claims recite subject matter which is neither disclosed nor suggested in Toda.

Claim 1, upon which claims 2-4 are dependent, recites a semiconductor device which allows an input signal thereto to select one of N operation modes, and operates in the one of N operation modes. The device comprises a selection circuit for selecting an operation mode from the N operation modes when the input signal indicates the operation mode, and for selecting a predetermined operation mode from the N operation modes when the input signal is an undefined signal indicating none of the N operation modes. An internal circuit operates in one of the operation mode and the predetermined operation mode selected by the selection circuit. Selection of the predetermined operation mode

prevents malfunction of the internal circuit when the input signal is the undefined signal.

Claim 5, upon which claims 6-10 are dependent, recites a semiconductor device which allows an input signal thereto to select one of N operation modes and operates in the one of the N operation modes. The device of claim 5 comprises a selection circuit for selecting an operation mode from the N operation modes when the input signal indicates the operation mode, and for selecting a predetermined operation mode from the N operation modes when the input signal is an undefined signal indicating none of the N operation modes. A core circuit is provided for storing data, and a control circuit operates in an operation mode selected by the selection circuit to control the core circuit.

As a result of the claimed configurations of the invention, a semiconductor device is provided wherein normal operation occurs even when undefined settings are made to mode registers, and wherein the internal circuit can be prevented from malfunctioning even when the input signal does not indicate any appropriate operation modes. Specifically, even when the input signal is an undefined signal, a predetermined operation mode is selected from existing operation modes. The internal circuit is then controlled in an appropriate matter. This configuration provides a reliable system for preventing malfunction of the semiconductor device. It is respectfully submitted that Toda fails to disclose or suggest the elements of the claimed invention, and therefore fails to provide the critical and unobvious advantages discussed above.

Toda discloses an operation mode setting circuit for DRAM, wherein operation modes can be selected by the CAS-BEFORE-RAS operation without reducing operation speed. A first buffer circuit is provided for converting a level of a mode setting signal

supplied from outside of the DRAM, and a second buffer circuit is provided for concerting the level of a CAS signal. A mode selection circuit is provided for latching and outputting a mode selection signal in response to output signals of the first and second buffer circuits, and a latching circuit is provided for receiving an address signal from outside of the DRAM and an address signal formed in an internal circuit, latching one of the received address signals in response to the mode selection signal from the mode selection circuit and the RAS signal, and then outputting the latched signal to the internal circuit. A control signal generation circuit generates a controlled signal for controlling the operation of the latching circuit based upon the RAS signal and the auto-refresh signal. However, Toda discloses a configuration wherein the mode selection circuit supplies a mode setting signal to the address buffer signal based upon an externally provided mode setting control signal; this, therefore, is a predetermined signal. Therefore, Toda is significantly different from the present invention, in that the present invention selects a mode from selectable modes when an undefined signal is input with no settings for mode selection. A goal in Toda is to achieve high-speed mode switching, while the present invention is intended to minimize or eliminate malfunction by securing stable operation of internal circuits, even when undefined signals are input. Therefore, it is respectfully submitted that there is no disclosure nor suggestion in Toda of the elements of either of claims 1 and 5, and that, therefore, Toda fails to provide the critical and unobvious advantages discussed above.

It is noted that no prior art rejections have been made to any of claims 2-4 and 6-11. As discussed above, applicant respectfully submits that these claims are in compliance with United States patent practice in that they particularly point out and distinctly claim the

subject matter of the invention.

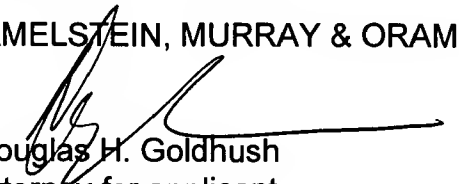
In view of the above, applicant respectfully submits that all of claims 1-11 recite subject matter which is neither disclosed nor suggested in the cited prior art. It is respectfully submitted that this subject matter is more than sufficient to render the claimed invention unobvious to a person of ordinary skill in the art. Applicant therefore requests that claims 1-11 be found allowable, and this application passed to issue.

If for any reason the Examiner feels the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 14-1060.

Respectfully submitted,

NIKAIDO, MARMELSTEIN, MURRAY & ORAM LLP



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